UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,430	03/03/2004	Michael P. Belyansky	FIS920030245	2429

29625 7590 07/25/2005

MCGUIRE WOODS LLP
1750 TYSONS BLVD.
SUITE 1800
MCLEAN, VA 22102-4215

EXAMINER
HUYNH, ANDY

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/708,430	BELYANSKY ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/28/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated June 27, 2005, Applicant has elected without traverse Invention I (Claims **1-25**), drawn to a method is acknowledged. Claims **26-30** are canceled. Accordingly, Claims **1-25** are pending in this application.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 06/28/2004. The references cited on the PTOL 1449 form have been considered.

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claims **1, 18, 19, 20 and 23** are objected to because of the following reasons.

In Claim **1**, line 2, "… between a gate a the mandrel layer;" should read –… between a gate and a mandrel layer;--, Claim **18**, line 3, "a stress imposing material" should read –the stress imposing material--, Claim **19**, line 7, "the spacer void" should read –the spacer voids--, Claim

20, the step of "filling a second portion of the recesses with a semiconductor material;" should be deleted. It is not necessary because it has already recited in Claim **19**, and Claim **23**, lines 14-16, "masking the first type of field effect transistor gate … and introducing stress material for the first type of field effect transistor gate" should read –masking the first type of field effect transistor gate … and introducing stress material for the second type of field effect transistor gate--.

Also, Claim **23** is object to because the claim contains subject matter which was not described in the specification and drawing.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1, 3-5 and 9-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (USP 6,111,292 hereinafter referred to as "Gardner") in view of Huang et al. (US Pub. No. 2005/0082522 A1 filed 07/23/2004, publication date: 04/21/2005, which claims benefit of the Provisional application No. 60/490,425, filed on July 25, 2003, hereinafter referred to as "Huang").

Regarding Claims **1, 3, 4, 10-13**, Gardner discloses in Figs. 7-11 and the corresponding texts as set forth in column 6, line 40-column 9, line 29, a method of forming a semiconductor structure comprises steps of:

forming spacer voids/openings 46 between a gate 44 and a mandrel/dielectric layer 34;

creating recesses/LDD areas 48 in a substrate 30 below and in alignment with the spacer voids/the openings; and

removing the mandrel/dielectric layer.

Gardner fails to teach a method of forming a semiconductor structure comprises steps of filling a first portion of recesses with a stress imposing material; and filling a second portion of the recesses with a semiconductor material; wherein the recesses include a first recess and a second recess, the first recess and the second recess having a depth greater than a depth of the bottom of a channel area of the gate, and wherein the first recess has a depth substantially equal to the depth of the second recess. Huang teaches in Fig 2c-2g and the correspond texts as set forth in paragraphs [0020]-[0031], a method of forming a strained channel device, comprises the steps of forming recesses 112 in a substrate 100; filling a first portion of recesses with a stress imposing material 114; and filling a second portion of the recesses with a semiconductor material 116, wherein the recesses include a first recess and a second recess, the first recess and the second recess having a depth greater than a depth of the bottom of a channel area 109 of the gate 119, and wherein the first recess has a depth substantially equal to the depth of the second recess. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of forming recesses in a substrate, filling a first portion of recesses with a stress imposing material, and filling a second portion of the recesses with a semiconductor

material, wherein the recesses include a first recess and a second recess, the first recess and the second recess having a depth greater than a depth of the bottom of a channel area of the gate, and wherein the first recess has a depth substantially equal to the depth of the second recess, as taught by Huang to incorporate into the Gardner's method and modify the Gardner's method to include the Huang's teachings to arrive the claimed limitations in order to provide a strained-channel transistor.

Regarding Claim **5**, Huang discloses the depth of the recess area is about 150 to 2000 angstroms. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the depth of the recess has a depth of about 500 to 2000 angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding Claim **9**, Gardner discloses in Fig. 9 the recesses/openings are substantially equidistant from the gate.

Regarding Claims **14 and 15**, Huang discloses the stress imposing material/the stress-inducing layer is made of silicon germanium ([0024], lines 1-2), and the semiconductor material is made of epitaxially grown Si ([0024], lines 3-4). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the stress imposing material/the stress-inducing layer made of silicon germanium, and the semiconductor material is made of epitaxially grown Si, as taught by Huang in order to provide a strained-channel transistor.

Regarding Claims **16 and 17**, Huang discloses the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress or a compressive stress. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress or a compressive stress since it was known in the art that the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate, and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

Regarding Claim **18**, Huang discloses a method further comprising a step of annealing after filling the first portion of the first recess and the first portion of the second recess with a stress imposing material ([0030]).

Claims **2 and 6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (USP 6,111,292 hereinafter referred to as "Gardner") in view of Huang et al. (US Pub. No. 2005/0082522 A1 filed 07/23/2004, publication date: 04/21/2005, which claims benefit of the Provisional application No. 60/490,425, filed on July 25, 2003, hereinafter referred to as "Huang") further in view of Yu (USP 6,297,117).

Regarding Claim **2**, Gardner and Huang disclose all the claimed limitations except for a method further includes forming dummy spacers between the mandrel layer and the gate and forming a nitride interface as an etch stop in the recesses. Yu teaches in Fig. 5 that a method for

forming a field effect transistor comprises forming dummy spacers 224, 226 between the mandrel/insulating layer 230 and the gate 208 and forming a nitride/liner oxide interface 228 (col. 5, lines 21-31). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form dummy spacers between the mandrel/insulating layer and the gate and forming a nitride/liner oxide interface, as taught by Yu in order to provide a smooth transition between the dummy spacers and the sidewalls of the gate structure (col. 5, lines 26-28).

Regarding Claims **6-8**, Gardner and Huang disclose all the claimed limitations except for a method further comprises forming dummy spacers and removing the dummy spacers to form the spacer voids, wherein: a first dummy spacer has a first width; a second dummy spacer has a second width; a first recess of the recesses has a width substantially equal to the first width of the first dummy spacer; and a second recess of the recesses has a width substantially equal to the second width of the second dummy spacer, wherein the first width is substantially equal to the second width; and wherein the first width is about 100 to1000 Å. Yu teaches in Figs. 5-6 that a method for forming a field effect transistor further comprises forming dummy spacers 224, 226 and removing the dummy spacers to form the spacer voids/openings 232, 234, wherein a first dummy spacer 224 has a first width; a second dummy spacer 226 has a second width, and wherein the first width is substantially equal to the second width (col. 5, line 50-col. 6, line 4). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form dummy spacers and removing the dummy spacers to form the spacer voids/openings, wherein a first dummy spacer has a first width; a second dummy spacer has a second width and wherein the first width is substantially equal to the second width, as taught by Yu to incorporate

into Gardner and Huang's methods to further include forming dummy spacers and removing the dummy spacers to form the spacer voids, wherein: a first dummy spacer has a first width; a second dummy spacer has a second width; a first recess of the recesses has a width substantially equal to the first width of the first dummy spacer; and a second recess of the recesses has a width substantially equal to the second width of the second dummy spacer since it was known in the art that processes for forming such first and second dummy spacers are known to one of ordinary skill in the art of integrated circuit fabrication (col. 28-31). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the first width is about 100 to1000 Å, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims **19-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (USP 6,297,117) in view of Gardner et al. (USP 6,111,292 hereinafter referred to as "Gardner") further in view of Huang et al. (US Pub. No. 2005/0082522 A1 filed 07/23/2004, publication date: 04/21/2005, which claims benefit of the Provisional application No. 60/490,425, filed on July 25, 2003, hereinafter referred to as "Huang").

Regarding Claims **19-20**, Yu discloses in Figs. 5-6 and the corresponding texts as set forth in column 5, line 50-column 6, line 4, a method of forming a semiconductor structure comprises steps of:

forming first dummy spacers 224, 226 on sides of a gate 208 formed on a substrate 204;

forming a mandrel/insulating layer 230 with portions of the mandrel/insulating layer abutting the dummy spacers; and

removing the dummy spacers to form spacer voids/openings 232, 234 between the gate and mandrel/insulating layer.

Yu fails to teach a method of forming a semiconductor structure comprises steps of creating recesses in the substrate below and in alignment with the spacer void; filling a first portion of the recesses with a stress imposing material; and filling a second portion of the recesses with a semiconductor material. Gardner discloses in Figs. 7-11 and the corresponding texts as set forth in column 6, line 40-column 9, line 29, a method of forming a semiconductor structure comprises steps of forming spacer voids/openings 46 between a gate 44 and a mandrel/dielectric layer 34; creating recesses/LDD areas 48 in a substrate 30 below and in alignment with the spacer voids/the openings, removing the mandrel/dielectric layer. Gardner fails to teach a method of forming a semiconductor structure comprises steps of filling a first portion of recesses with a stress imposing material; and filling a second portion of the recesses with a semiconductor material. Huang teaches in Fig 2c-2g and the correspond texts as set forth in paragraphs [0020]-[0031], a method of forming a strained channel device, comprises the steps of forming recesses 112 in a substrate 100; filling a first portion of recesses with a stress imposing material 114; and filling a second portion of the recesses with a semiconductor material 116. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of forming recesses in a substrate, filling a first portion of recesses with a stress imposing material, and filling a second portion of the recesses with a semiconductor material, as taught by Huang to incorporate into and modify the Yu and

Gardner's method to include the Huang's teachings to arrive the claimed limitations in order to provide a strained-channel transistor.

Regarding Claim **21**, Huang discloses the stress imposing material/the stress-inducing layer is made of silicon germanium ([0024], lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the stress imposing material/the stress-inducing layer made of silicon germanium, as taught by Huang in order to provide a strained-channel transistor.

Regarding Claims **22 and 25**, Huang discloses the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress or a compressive stress. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress or a compressive stress since it was known in the art that the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate, and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

Regarding Claims **23-24**, the rejection would be the same as the rejected Claim **19** with a first type of field effect transistor gate and a second type of field effect transistor gate.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

07/21/05

Andy Huynh

Patent Examiner